REMARKS/ARGUMENTS

Claims 1-14, 18, 20-24 and 26-31 are pending in this application. Claims 18 and 20-23 are allowed. Claims 1-3, 5-10, 12-14, 24 and 26-31 are rejected. Claims 8-10 and 12-14 are rejected under 35 U.S.C. §102(e) as being anticipated by Chin et al. (U.S. Patent 6,202,101). Claims 1-3, 5-7, 24 and 26-31 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Chin et al. (U.S. Patent 6,202,101). Applicants gratefully acknowledge the Office Action's indication that claims 18 and 20-23 are allowed and that claims 4 and 11 are allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Claims 8 and 24 are amended to bring the claims into better form.

Applicant respectfully submits the cited reference does not teach, suggest or disclose at least "[a] graphics device comprising: ... a multipurpose buffer mechanism to simultaneously monitor a status of said plurality of data requests..." (e.g., as described in claim 1).

In its rejection of claims 1 and 8, the Office Action asserts that Chin teaches a multipurpose buffer mechanism in that "bus interface unit 14 includes processor controller 42 in Fig. 2 and further having in-order queue 64, peripheral queue 66, and memory queue 68 in Fig. 4". Applicants respectfully disagree and submit these elements do not describe the relevant limitations.

First, Applicants submit that cited element "bus interface unit" 14 is used interchangeably with the term "interface controller" 14. However, as is well known to those of ordinary skill in the art a *controller* is not the same thing as a *buffer*, and each are directed toward different purposes. The controllers cited in the Office Action are directed

toward transferring data, function dissimilar to that of a buffer. Therefore, neither the bus interface unit/interface controller nor the processor controller 42 are sufficient to disclose "a multipurpose buffer mechanism to simultaneously monitor a status of said plurality of data requests" as described in embodiments of the present application.

Next, the Office Action cites in-order queue 64, peripheral queue 66, and memory queue 68 (as part of processor controller 42) illustrated in Figure 4. However, as indicated in their names, each of these elements is directed toward a specific, individual task. For example, column 11, lines 15-22 state:

> The entry number 0 is stored in the in-order queue 64 and either in queue 66 or queue 68 depending on whether that request is a peripheral request or a memory request. If it is a memory request, then the entry number 0, as well as the memory address, will be loaded into queue 68, and not queue 66.
> A decoder is used to ascertain whether a request will be targeted for queue 66 or queue 68...

Therefore, as seen in the example above, each of these buffers is intended to have a separate purpose that operates conditionally. An examination of cited Figure 4 emphasizes this point. Each of these queues 64, 66 and 68 are *separate* elements with separate and distinct functions.

The illustration of Figure 2 further emphasizes that the Chin reference does not describe the relevant limitations. Figure 2 describes the cited bus interface unit/ interface controller 14. Column 8, lines 30-44 state:

> FIG. 2 illustrates nine queues: processor-to-memory queue (P2M queue) 50a, processor-to-PCI/AGP queue (P2I/A queue) 50b, memory-to-processor queue (M2P queue) 50c, memory-to-PCI queue (M2I queue) 50d, PCI-to-memory queue (I2M queue) 50e, PCI/AGP-to-processor queue (I/A2P queue) 50f, AGP-to-memory queue (A2M queue) 50g, memory-to-AGP queue (M2A queue) 50h, and PCI-to-AGP queue (I2A queue) 50i. It is recognized, that if needed, an additional graphics interface (i.e., GCI) beyond AGP can be used for graphics intensive

> applications. *Each of the queues 50 shown in FIG. 2 communicate with each other through the various controllers and/or control signals routed directly between respective queues. (emphasis added)*

Therefore, as further shown in the description of Figure 2, the queue elements of Chin each have a specific, individual purpose and operate together. Applicants submit the in-order queue 64, peripheral queue 66, and memory queue 68 included as part of a *processor controller* are insufficient to describe *a multipurpose buffer mechanism to simultaneously monitor a status of said plurality of data requests* (e.g., as described in claim 1).

Therefore, since each and every element of claim 1 is not taught, suggested or disclosed by the cited reference, Applicant respectfully submits that the §103(a) rejection is lacking and should be withdrawn. Likewise, claim 8 includes similar limitations and therefore the §102(e) rejection should be withdrawn. Claims 2-3, 5-7, 9-10 and 12-14 depend from and further define allowable independent claims 1 and 8, and therefore are allowable as well.

Applicants further submit that the Chin reference does not teach, suggest or disclose "[a] method comprising: ...obtaining data regarding said plurality of data requests from a plurality of memory devices ... wherein obtaining said data comprises monitoring a status of a plurality of operations regarding said plurality of data requests" (e.g., as described in claim 24).

The Office Action states Chin teaches each request queue of Chin may be a circular FIFO buffer or may have I/O points which indicate the I/O locations, and thus

their status can be seen from the location of the circular FIFO or their pointers (citing column 3, lines 44-64). Column 3 lines 44-64 state:

> *According to one embodiment, each request queue may be a circular first-in-first-out ("FIFO") circular buffer, or may have input and output points which indicate the input location or "head" of a series of filled locations and an output location or "tail" which tags the culmination of the series of filled locations.*
> *Among information stored within the peripheral and memory request queues are addresses as well as the type of request being solicited (i.e., whether the request is to memory or a peripheral device, or is a read request or a write request).* An entry number may be used within the memory request queue to resolve coherency with a snoop result to cache. *According to another embodiment, entry numbers may also be associated with the peripheral request queue to note the relative order in which requests are placed within each queue and among both queues if, for example, the requests are placed in the respective queues out-of-order.* The entry numbers need not be employed in the peripheral request queue (and memory request queue) if the requests are issued to the respective queues in-order and maintained in-order within respective memory and peripheral data queues containing the responses to the respective requests. *(emphasis added)*

Applicants submit the first italicized section of the cited section describes keeping using *memory locations* (including the first location "head" and last location "tail" when the locations are full) to store information. Contrary to the Office Action's assertion, monitoring the memory locations that are being used in a "head" to "tail" fashion is not the equivalent of *monitoring the status of monitoring a status of a plurality of operations regarding said plurality of data requests.*

Next, the first italicized section further describes the operation of *peripheral and memory request queues* (not the FIFO circular buffer described just above). These queues store information such as addresses and the type of request being solicited. The final italicized section describes noting the relative order in which requests are placed. However, again, these queues do not *monitor the status of monitoring a status of a*

plurality of operations regarding said plurality of data requests as described in embodiments of the present application.

For at least the above reasons, Applicants submit that the cited sections are inadequate to support a proper §103(a) rejection of independent claim 24, and claim 24 should be allowed. Claim 28 contains similar allowable limitations and therefore should be allowed as well. Claims 26-27 and 29-31 are allowable for depending from allowable base claims.

For at least all the above reasons, the Applicants respectfully submit that this application is in condition for allowance. A Notice of Allowance is earnestly solicited.

The Examiner is invited to contact the undersigned at (408) 975-7500 to discuss any matter concerning this application. The Office is hereby authorized to charge any additional fees or credit any overpayments under 37 C.F.R. § 1.16 or § 1.17 to Deposit Account No. **11-0600**.

Respectfully submitted,

KENYON & KENYON LLP

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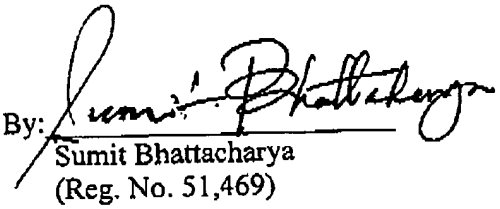
By: 
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